What is claimed is:

1. An optical detecting module comprising:

a silicon substrate where a cavity is formed at a middle portion thereof;

an aperture membrane formed on the cavity of the silicon substrate and provided with an optical aperture for passing light; and

an array of photodiodes formed at an upper surface of the silicon substrate for receiving light emitted from a light source and an optical signal reflected from an optical disc and converting into an electric signal for detection.

2. The optical detecting module of claim 1, further comprising a reflective thin film at an upper surface of the aperture membrane.

3. The optical detecting module of claim 1, wherein the array of the photodiodes comprises:

a common ground electrode;

an emitted laser beam monitoring photodiode for monitoring an optical output from a light source and maintaining the optical output as a predetermined level through a feedback control circuit;

radio frequency signal detecting photodiodes having data information included in an optical signal reflected from a recording layer of the optical disc; and

photodiode segments arranged right and left by being divided into six regions for detecting information of a focus shape and a focus depth of laser beam irradiated on the optical disc substrate.

4. The optical detecting module of claim 1 or 3, wherein each photodiode is a semiconductor P-N junction diode or a P-I-N junction diode.

5. The optical detecting module of claim 1, wherein a spacer is installed at both ends of an upper surface of the silicon substrate.

6. The optical detecting module of claim 4, wherein the spacer is soda lime glass containing Na of a certain concentration.

7. A light emitting module comprising:

an SOI substrate of a plate type provided with a silicon dioxide film between an upper silicon layer and a lower silicon layer;

an electrode metal pad attached to a part where the upper silicon layer is stripped among an upper surface of the SOI substrate;

a laser diode attached to an upper surface of the electrode metal pad; and

a mirror slantly formed at one side of the upper silicon layer with 45° for reflecting light emitted from the laser diode.

8. The light emitting module of claim 7, wherein a spacer is bonded at both ends of the upper surface of the SOI substrate.

9. The light emitting module of claim 8, wherein the spacer is soda lime glass.

10. An optical pickup apparatus comprising:

a light emitting module comprising an SOI substrate of a plate type provided with a silicon dioxide film between an upper silicon layer and a lower silicon layer, an electrode metal pad attached to a part where the upper silicon layer is stripped among an upper surface of the SOI substrate, a laser diode attached to an upper surface of the electrode metal pad, and a mirror slantly formed at one side of the upper silicon layer with 45° for reflecting light emitted from the laser diode;

an optical detecting module comprising a silicon substrate arranged at an upper portion of the light emitting module and provided with a cavity at a middle portion thereof, an aperture membrane formed on the cavity of the silicon substrate and provided with an optical aperture for passing light at a center portion thereof, and a photo diode formed at an upper surface of the silicon substrate for converting light emitted from the laser diode and an optical signal reflected from an optical disc and having information into an electric signal for detection; and

a spacer bonded between the light emitting module and the optical detecting module for uniformly maintaining a gap therebetween.

11. A method for manufacturing an optical detecting module comprising:

a first step of patterning a photosensitive film on a silicon substrate by using a silicon substrate of {100} crystal direction doped with n-type impurities as a starting material thus to form an opening window for injecting p type impurities, injecting the p type impurities into the opening window by using the photosensitive film as a mask, and stripping the photosensitive film and performing a thermal process for annealing and diffusion thus to form an intrinsic well;

a second step of patterning a photosensitive film on the silicon substrate thus to form the p type impurities at a partial region of the intrinsic well, stripping the photosensitive film and performing a thermal process for annealing and diffusion thus to form a photodiode p type junction, and completing a photodiode of an p-I-n junction structure by a thermal process;

a third step of respectively depositing multi-layered thin films of a three-layer structure of silicon dioxide film/ silicon nitride film/ silicon dioxide film at upper and lower surfaces of the silicon substrate where the photodiode is completed, stripping a part which has not been covered by the photosensitive film among the multi-layered thin film formed at the upper surface of the silicon substrate by using a photosensitive film patterned by a photolithography process as an etching mask, and then stripping the photosensitive film;

a fourth step of depositing a metal thin film in order to form a photodiode and a reflective thin film on the silicon substrate, patterning a photosensitive film at a surface of the deposited metal thin film by a photolithography process, then selectively stripping the metal thin film by using the photosensitive film as an etching mask, then stripping the photosensitive film, and thereby forming a photodiode metal electrode wire, a metal electrode pad, and the reflective thin film;

a fifth step of depositing a metal thin film on the silicon substrate and then partially etching the etching mask thin film located at a part where an optical aperture will be formed by a photolithography process and a thin film etching technique;

a sixth step of patterning a photosensitive film at a lower surface of the silicon substrate thus to align the photosensitive film with an aperture membrane formed on a wafer, patterning an etching mask thin film at a lower surface of the

silicon substrate by using the photosensitive film, and stripping the photosensitive film thus to obtain an etching region which will be processed in the next step by a wet anisotropy silicon etching technique;

a seventh step of etching silicon of a lower surface of the substrate exposed through the etching mask thin film by impregnating with aqueous anisotropic silicon etchant thus to form a cavity;

an eighth step of stripping a multi-layered thin film exposed through the etching mask thin film formed at an upper surface of the silicon substrate by a reactive ion etching, and stripping the mask thin film thus to complete the optical aperture; and

a ninth step of bonding a spacer formed of glass material with the silicon substrate as a wafer form, and dicing as an individual chip unit.

12. The method of claim 11, wherein either boron or BF_2 is used as the p type impurities in the first step.

13. The method of claim 11, wherein a low stress silicon nitride is respectively deposited at upper and lower surfaces of the silicon substrate by a chemical vapor deposition method in the third step.

14. The method of claim 11, wherein multi-layered thin films having a three-layer structure of silicon dioxide film/ silicon nitride film/ silicon dioxide film are respectively deposited at the upper and lower surfaces of the silicon substrate in the third step.

15. The method of claim 11, wherein the photosensitive film is patterned at the lower surface of the silicon substrate by using a both-surface aligning technique in the sixth step.

16. The method of claim 11, wherein the aqueous anisotropic silicon etchant is one of KOH (potassium hydroxidation film), NaOH, TMAH (tetra-methyl ammonium hydroxidation film), and EDP (ethylenediamine pyrocatecol) in the seventh step.

17. A method for manufacturing a light emitting module comprising:

a first step of preparing an SOI substrate as a starting material and respectively forming mask thin films such as a silicon nitride film or a silicon dioxide film which are not etched by anisotropic silicon ethant and which will be used as an anisotropy silicon etching mask layer at upper and lower surfaces of the SOI substrate;

a second step of coating a photosensitive film on a surface of the etching mask thin film formed on an upper silicon layer of the SOI substrate, pattering the photosensitive film by a photolithography process, and stripping the exposed etching mask thin film with a reactive ion etching technique by using the photosensitive film as an etching mask thus to define an anisotropic etching region and strip the remaining photosensitive film;

a third step of etching the upper silicon layer exposed through the etching mask thin film by impregnating with anisotropic silicon etchant thus to firstly stop the etching at {111} crystal plane of the upper silicon layer and then to secondly stop the etching at a silicon dioxide film, and stripping the mask thin films of the

upper and lower surfaces of the SOI substrate used as an etching mask after the anisotropic silicon etching processing;

a fourth step of coating a thick photosensitive film on a surface of the upper silicon layer where a crystal plane is formed, patterning by a photolithography, and depositing a metal thin film on the patterned photosensitive film;

a fifth step of melting the thick photosensitive film in organic solvent by impregnation, stripping the photosensitive film and the metal thin film formed on the photosensitive film, and leaving the metal thin film only at a predetermined region of the SOI substrate on the oxidation film where the photosensitive film did not exist thus to form an electrode metal pad; and

a sixth step of aligning/ assembling a spacer for an alignment/ assembly with the SOI substrate where a mirror and the electrode metal pad are formed, then dicing as an individual chip unit, and then aligning the laser diode with the electrode metal pad by using a solder bonding technique.

18. The method of claim 17, wherein the anisotropic silicon etchant is one of KOH, TMAH, EDP, and NaOH in the third step.

19. . The method of claim 17, wherein the {111} crystal plane, an etching remaining surface formed after etching the upper silicon layer having a surface slantly polished with 9.74° for a {100} crystal plane has a crystal plane having an inclination of 45° for a surface of the SOI substrate, and another etching remaining surface, a {111} crystal plane facing the inclination surface has an inclination of 64.48° for the surface of the substrate in the third step.

20. The method of claim 17, wherein the glass has crystal planes having an inclination of 45°.

21. The method of claim 17, wherein the spacer is bonded with the SOI substrate by using one of an anodic bonding and an epoxy resin bonding in the sixth step.